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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,343	11/18/2003	Schuyler E. Shimanek	X-1414 US	8186

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EXAMINER	
TAN, VIBOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,343	SHIMANEK ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-17,22 and 24-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8,9,12-17,22 and 24-28* is/are rejected.

7)☒ Claim(s) *7,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 12-17, 22, 24, 26 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (U. S. PAT. 5,487,037).

In claim 1, Lee teaches all claimed features in Fig. 11, a memory array comprising: a bitline (C); and a plurality of memory cells (RAM/ROM hybrid cells, abs.), each of the plurality of memory cells having: a configuration bit terminal (not shown but would be an input/output line coupled to an input of 1110, inherent); a pair of cross-coupled inverters (1110s) having first and second bit nodes (cross-coupled nodes), wherein one of the first and second bit nodes is connected to the configuration bit terminal (not shown but would be a line coupled to the input/ouput of 1110s, inherent); an access transistor (1120) having a first current-carrying terminal (drain terminal) connected to the bitline, a second current-carrying terminal (source terminal) connected to the first bit node, and an access-transistor control terminal (gate terminal coupled to ROW); and a memory transistor (1140) having a first current-carrying terminal (drain) connected to one of the first and second bit nodes, a second current-carrying terminal (source terminal) connected to a power supply node (ground), and a memory-transistor control terminal (gate terminal coupled to RE); wherein each of the plurality of memory

cells further includes a programmable interconnection (1130) interposed between the first current-carrying terminal (the drain terminal of 1140) of the memory transistor and at least one of the first and second bit nodes (the cross-coupled nodes).

In claim 2, Lee further teaches the memory array of claim 1, further comprising a second configuration bit terminal (would be a second output line coupled to an output of 1110, inherent) connected to the first bit node, wherein the first- mentioned configuration bit terminal connects to the second bit node.

In claim 8, Lee teaches all claimed features in Fig. 11, a memory array comprising: a bitline (C); and a plurality of memory cells (RAM/ROM hybrid cells, abs.), each of the plurality of memory cells having: a configuration bit terminal (not shown but would be an output line coupled to an input of 1110, inherent); a pair of cross-coupled inverters (1110s) having first and second bit nodes (cross-coupled nodes), wherein one of the first and second bit nodes is connected to the configuration bit terminal (not shown but would be a line coupled to the input/output of 1110, inherent); an access transistor (1120) having a first current-carrying terminal (drain terminal) connected to the bitline, a second current-carrying terminal (source terminal) connected to the first bit node, and an access-transistor control terminal (gate terminal coupled to ROW); and a memory transistor (1140) having a first current-carrying terminal (drain) connected to one of the first and second bit nodes, a second current-carrying terminal (source terminal) connected to a power supply node (ground), and a memory-transistor control terminal (gate terminal coupled to RE); wherein each of the plurality of memory cells further includes a programmable interconnection (1130) interposed between the second

current-carrying terminal (the source terminal of 1140) of the memory transistor and at least one of first and second power supply nodes (ground).

In claim 4, Lee further teaches the memory array of claim 1, the access-transistor control terminal receiving at least one of a read control signal and a write control signal (ROW).

In claims 12-14, Lee further teaches the memory array of claim 1, wherein the cross-coupled pair of inverters (1110s) is part of a static random-access memory (SRAM) cell (abs.); wherein the memory transistor is part of a read-only memory (ROM) cell (abs.); and wherein the memory array is part of a configuration memory of a programmable logic device (title).

In claim 15, Lee further teaches the memory array of claim 1 comprising a memory control terminal (a gate terminal of 1140 coupled to the gate terminal of the other 1140) connected to the memory transistor control terminals, the memory control terminal having first (RE is 1) and second (RE is 0) states, wherein the first state configures the memory cells as read-only memory (col. 10, line 12) and the second state configures the memory cells as random-access memory (col. 10, line 8).

In claim 16, Lee further teaches the memory array of claim 15, wherein the circuit is part of a configuration memory of a programmable logic device, and wherein the first state of the memory control terminal (when RE 1) renders the programmable logic device an application specific circuit (ASIC).

In claim 17, Lee further teaches the memory array of claim 1, wherein the power supply node is ground (as shown).

In claim 22, Lee teaches all claimed features in Fig. 11 and column 2 lines 3-9, a circuit comprising: a plurality of memory cells (RAM/ROM), each memory cell supporting a random- access memory mode and a read-only memory mode (RAM/ROM hybrid); and an array of configurable logic resources (inherent; would be I/O logic circuits coupling to the input/outputs of the memory cells) connected to the memory cells: wherein each memory cell includes a mode switch selecting one of the random-access memory mode or the read-only memory mode (col. 10, lines 5-11).

In claim 24, Lee further teaches the circuit of claim 22, wherein each memory cell includes a random-access memory cell and a read-only memory cell (Fig. 11).

In claim 26, Lee teaches all claimed features in Fig. 11, a programmable logic device comprising: configurable logic resources (inherent; would be I/O logic circuits coupling to the input/outputs of the memory cells) having a plurality of configuration bit terminals (input/output terminals of cross coupled 1110s); and a plurality of memory cells (cross coupled 1110s), each memory cell including: a configuration bit node (one of cross coupled bit nodes) connected to one of the plurality of configuration bit terminals of the configurable logic resources and providing a configuration-bit signal (supplied by the would be I/O logic circuits coupling to the input/outputs of the memory cells; inherent); a random-access memory element (one of RAM/ROM hybrid cells used as RAM element); a read-only memory element (one of RAM/ROM hybrid cells used as ROM element); and at least one memory control terminal (RE) selecting one of the random-access memory element and the read-only memory element to control the configuration-bit signal.

In claim 28, Lee further teaches the programmable logic device of claim 26, wherein the random- access memory element is a static random-access memory element (SRAM; abs.).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Zhang et al (U. S. PAT. 5,986,923).

In claim 3, Lee teaches the memory array of claim 1, with the exception of teaching a configurable resource connected to the configuration bit terminal, the configuration terminal transmitting a configuration voltage to the configurable resource. However, Zhang et al. teaches in Figs. 1 and 2, a configurable resource (I/O ports 112, 114) connected to the configuration bit terminal (D1' or D1), the configuration terminal transmitting a configuration voltage to the configurable resource (col. 3, lines 1-3 and 58-60).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Lee with the teachings of Zhang et al. to force the configurable resource, I/O ports in Zhang, to the selected logic voltages, which are maintained as long as power is supplied to the memory cell, or until the memory is rewritten.

5. Claims 6, 9, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Raza (U. S. PAT. 5,943,488).

In claim 6, Lee teaches all claimed features the memory array of claim 1; with the exception of teaching wherein each of the plurality of the memory cells further includes a mask-programmable interconnect providing the programmable interconnection. However, Raza teaches in Figs. 7-8 and in column 2, lines 45-47 a mask programmed or programmable cell and the implementation of the interconnect map on the mask programmable device or array by mask programming the interconnects determined in the interconnect map onto the mask programmable device or array.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to include a mask-programmable interconnect, as taught by Raza, in the plurality of memory cells of Lee, in order to provide mask programmable chips that may be faster and may consume less power than fully programmable PLDs and yet are derived from programmable PLD's such that redesign of the mask programmable device merely involves re-programming of the programmable device to derive the mask for the mask programmable device.

Claim 9 is rejected in the same manner as claim 6.

In claim 25, Lee teaches all claimed features the circuit of claim 24; with the exception of teaching wherein the read-only memory cells are mask programmable. However, Raza teaches in Figs. 7-8 and in column 2, lines 45-47 a mask programmed or programmable cell and the implementation of the interconnect map on the mask

programmable device or array by mask programming the interconnects determined in the interconnect map onto the mask programmable device or array.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to include a mask-programmable interconnect, as taught by Raza, in the plurality of memory cells of Lee, in order to provide mask programmable chips that may be faster and may consume less power than fully programmable PLDs and yet are derived from programmable PLD's such that redesign of the mask programmable device merely involves re-programming of the programmable device to derive the mask for the mask programmable device.

In claim 27, Lee teaches all claimed features the programmable logic device of claim 26; with the teaching of wherein the read-only memory element is mask programmed.

However, Raza teaches in Figs. 7-8 and in column 2, lines 45-47 a mask programmed or programmable cell and the implementation of the interconnect map on the mask programmable device or array by mask programming the interconnects determined in the interconnect map onto the mask programmable device or array.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to include a mask-programmable interconnect, as taught by Raza, in the plurality of memory cells of Lee, in order to provide mask programmable chips that may be faster and may consume less power than fully programmable PLDs and yet are derived from programmable PLD's such that redesign of the mask

programmable device merely involves re-programming of the programmable device to derive the mask for the mask programmable device.

6. Claims 7, 10 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 22 and 26 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER